INFORMATION DISCLOSURE CITATION

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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
K	5,614,855	03-25-97	Lee et al.	327	—	
K	5,554,945	09-10-96	Lee et al.	327	—	
K	5,513,327	04-30-96	Farmwald et al.	395	—	
K	5,485,490	01-16-96	Leung et al.	375	—	
K	5,432,823	07-11-95	Gasbarro et al.	375	—	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

K	"A Semidigital Dual Delay-Locked Loop" ; Stefanos Sidiropoulous; IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997
K	"A 2Gb/s/pin CMOS Asymmetric Serial Link"; Chang et al; 1998 Symposium on VLSI Circuits Digest of Technical Papers

EXAMINER	DATE CONSIDERED
Kevin Kim	5/5/03

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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